

The Defense Advanced Research Projects Agency, Information Technology Office intends to develop a new program in the area of computing systems that will provide unprecedented capabilities for dynamic adaptation of information systems to threats and rapidly evolving mission requirements of the Department of Defense. This program titled Adaptive Computing Systems will develop the COTS hardware components, design, programming, and runtime environments to enable an application to reach through to the hardware layer and directly manipulate the datapath-level architecture at runtime to optimize the application-level performance. The choice of the Chameleon metaphor reflects the unique ability of the technology to adapt to its environment.



### **Vision**



#### **Defense Environment**

- 30-year military vs. 18-month commercial product cycles
- New platforms equipped with 10-year old technology at time of deployment
- Numerous information technology subsystem improvement cycles
- · Proprietary, stovepiped systems
- Highly volatile COTS marketplace with little interest in defense problems

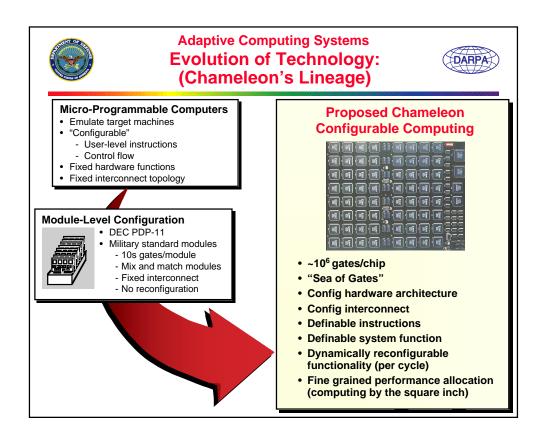
### **CHAMELEON**

Adaptive computing and communications technology for evolving Defense systems

- · Dynamic adaptation to threats
- Extended mission capabilities on existing platforms
- Seamless, complete, life cycle performance upgrades for whole system
- Commodity technology easily augmented to meet defense needs (i.e., fault tolerance, security, evolvability)



The Adaptive Computing Systems Program (ACS) operates in a Defense environment where affordability concerns are driving the adoption of open standards and COTS technology while the complexity of future missions is driving the need for dramatic improvements in system performance. These potentially conflicting goals are addressed by creating a novel computing system technology base that enables future Defense platforms to adapt to evolving threat and mission requirements. ACS will deliver a COTS, seamless computing environment in which resources can be dynamically allocated as well as easily extensible and upgradeable to enhance the capability of existing platforms. ACS technology will allow essential Defense enhancements like security and fault tolerance to be easily added to an underlying COTS technology system.



The concept of configurable computers dates back to at least the early 1970s when computers were assembled from a set of low-complexity hardware modules that were plugged into a backplane and wired to provide the desired computer architecture. These systems were "configured" by the selection of the appropriate hardware module. The Military also adopted a similar concept where families of Standard Electronic Modules were created and used across several systems. "Configuration" was again provided by mix-and-match selection of appropriate hardware modules. Specialized computer systems were also created to emulate other target computer systems. These microcoded machines enabled the creation of user-level instructions of various emulated machine architectures. These systems were configurable in the sense that although the underlying datapath and hardware functions were fixed they could be re-allocated to various target instructions. The ACS program will develop a hardware component base with module-level complexity as high as five orders of magnitude more complex than these early configurable systems.

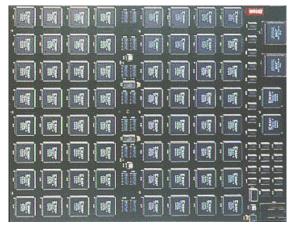
Systems which enable the application to reach through to the lowest level of hardware and manipulate the datapath at runtime. ACS will create the notion of computing by the square inch. An application will use as much hardware resource as it needs at each particular instant in time.



### **Adaptive Computing Systems** Complex System Hardware Emulation: (DARPA) The Technology Baseline for Chameleon



### State of the Art



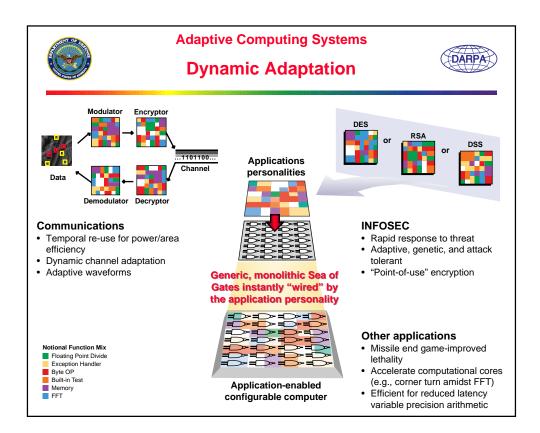
**Sponsor: DARPA Microsystems Program** 

**Performer: Virtual Machine Works** 

**Project: Virtual Wires** 

- 1M total gates
- 225K emulation gates
- 0.5 MHz emulation rate
- 6-8x cost reduction through "virtual wires" and direct connections
- 4 Mbits modular memory
- Pentium Pro emulation in 2-3 boards

Many of the programmable components delivered to the commercial market today are aimed at replacing a few integrated circuits on a printed circuit board with a programmable component. These components (i.e., Field Programmable Gate Arrays) are also used to create programmable systems designed to emulate complex integrated circuits such as microprocessors and ASICs. One such emulation system is produced by Virtual Machine Works resulting from a DARPAsponsored research project. This state-of-the-art system is able to emulate integrated circuits of the complexity of a Pentium (TM) processor with 2-3 logic boards. While these components form the technology base for configurable computing systems they are not optimized for computation but for emulation. New component architectures will be investigated that not only leverage the existing emulation technology but drive it toward the complex computational demands of Defense systems.



The ability to dynamically adapt is a critical attribute of future Defense systems. Adaptation may take the form of various phases of computation that are successively swapped into a configurable system for execution as in the example of a communications system. Other applications of dynamic behavior include the ability to rapidly adopt a new crypto algorithm in response to threat or to change the model of computation or algorithm family as a missile closes on a target.



## Adaptive Computing Systems Configurable Computing Systems: State of the Art



### **Laboratory Prototype Systems**

Algorithm         System         System         Speedup           Region labeling         Splash 2         Sparc 10         17           Genetic algorithm (TSM)         Splash 2         125MHz HP         10.5           DNA sequencing         Splash 2         MP-1 (8KPE)         65.6           Monte-Carlo 8x8         MCCP         ADSP-2101         14           Ising         Cellular Automata         CAFCA         Cray 2         1           PDE         RSA         PAM         150MHz Alpha         17.8           Cryptography         Template-based ray casting         RIPP-10         75MHz Pentium         33.8 Pentium           Median filter         Splash 2         Sparc 10         130           Fractal compression         Un-named         RS6000/340         50           FIR 8-bit 16 tap         1 Xilinx         50MHz DSP         17.88		Configurable Computer	Conventional Computer	
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- Interesting speedups on highly tuned, narrowly focused applications
- One of a kind lab systems owned by a research group
- Tools are reinvented for each specific machine
- No possibility of application portability
- Primitive or non-existent runtime environments
- Extremely difficult to program
- Compilation times from days to weeks to months

Technology maturity equivalent to the ENIAC

Adaptive or configurable computing systems have existed in various instantiations over about the last 10 years. These various computing systems have been essentially captive by the team that developed them. While showing promising results in narrowly-focused application areas they have not emerged from the laboratory to have any significant impact on computing. Lack of common software environments compounded by extremely long compilation times make these previous attempts very difficult to program by even the team that developed them. These symptoms are typical of a form of computing that is in its infancy. Recent events such as the first commercial offerings, likely dramatic improvements in component technology, and isolated demonstrations of very promising but preliminary results on critical Defense applications are leading indicators that ACS will be able to focus the research community, increase the awareness of the Defense agenda, and pull together industrial participation to deliver dramatic technology benefits to Defense over the next 5-10 years.



### **Chameleon Motivation**



### **Mechanisms**

- Exploit reconfiguration to redefine the boundary between hardware and software
- Provide configurable hardware abstraction to the algorithm design process; enables high level tradeoffs
- Optimize implementation through concurrent hardware/software design
- Define the hardware architecture dynamically at runtime (late binding)

### **Implications**

- Direct hardware instantiations of variable precision arithmetic
  - Core computations of signal/image processing
  - Orders of magnitude faster than software emulation
  - Efficient replacement of legacy systems (e.g., 18-bit computers)
- Defense enhancements to general purpose computation
  - Specialized instructions (e.g., pop count, bit matrix multiply, integer divide for public key encryption)
  - Instant instantiation of hardware function accelerators
    - MPEG or various video compression standards
    - High BW encryption (diverse standards)

Adaptive Computing Systems provides the ability to redefine the hardware/ software boundary in computing systems. This paradigm change is likely to produce new models of computation, new programming methods, and new approaches to algorithmic implementation. Some of the greatest gains in this field may well come from providing the appropriate abstractions of this technology to mathematicians and algorithm developers to allow them control over hardware "knobs" that have been previously denied. There are many implications of this new technology including the efficient redesign of obsolete systems including ones with unusual word lengths, and the ability to efficiently add instructions implemented in hardware to accelerate critical computations in relatively low-cost systems.



# Adaptive Computing Systems Chameleon Anticipated System-Level Benefits





 Continuous, sustained 100x performance improvement over microprocessing alternatives on critical defense signal processing applications (e.g., compression, search, matching, encryption)



- Cost-effective Defense Chameleon components available from high-volume commercial manufacturing
- Reduced life cycle costs, simplified logistics, fewer unique part types



- Seamless evolvable systems approach for extended lifetime platforms
- Uniform integration of currently disparate on-board systems
- Fault tolerance and graceful degradation through adaptation



 Algorithm development environment directly manipulates hardware architecture resulting in unprecedented efficiency (e.g., shorter development cycle, higher performance, reduced power consumption, reduced weight)

ACS technology promises to deliver increased performance at lower cost to Defense applications. Highly adaptable technology will provide improved efficiency in such diverse dimensions as power consumption, weight, time to deployment, and resource utilization.

### Representative Defense Applications

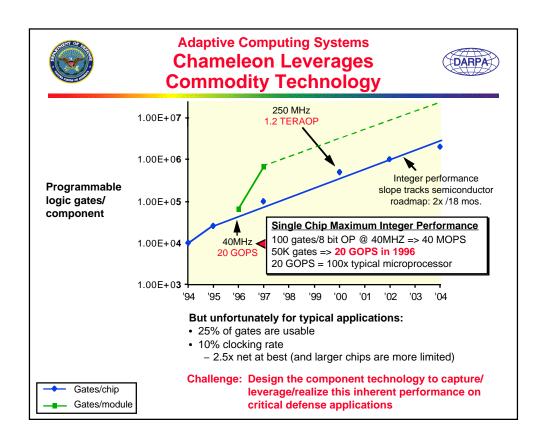


- Highly efficient co-processing (e.g. link encryption, protocol, compression, search, video, graphics, design)
- Limited production Defense embedded real-time computing systems
- INFOSEC, IW, security, SIGINT (e.g. wartime modes, remote denial of service, point-of-use instantiation of crypto services)
- GloMo intelligent, high-performance untethered C3 nodes as robust, highly adaptive elements of the mobile battlespace
- Highly adaptive robots providing intelligence/awareness in the distributed digital battlefield
- Remote, fielded system enhancement (e.g. bug fixes, new functionality, application-specific customization, security)
- Potential for mass market applications in general purpose computing

Adaptive Computing Systems technology will have broad impact across a number of Defense application areas, principally in the areas of signal and image processing and information security. The ultimate challenge for this technology is to supplant microprocessors in mainstream computing applications. While a total replacement of microprocessors is unlikely, it is an ACS goal to investigate new hybrid architectures that blend the strongest characteristics of both approaches to form new classes of architectures to meet Defense needs.

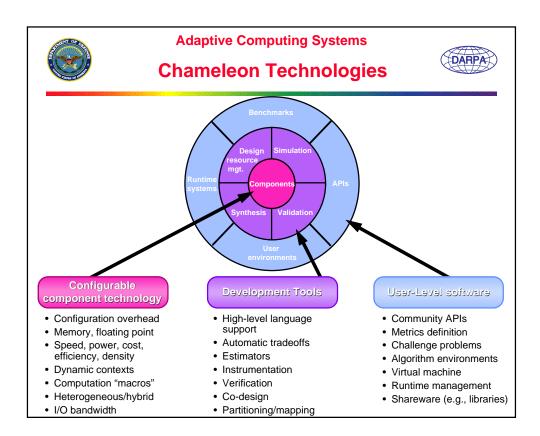


ACS faces a number of significant technical challenges across a broad range of issues. ACS will establish a research community of university, industry, and Defense participants to aggressively push these issues from a coordinated front. Significant progress is required in these areas to bring the technology to viable commercial practice and establish a stable low-cost source of technology for Defense.



Unlike many custom solutions, ACS technology rides the commodity semiconductor curves providing a 2x improvement in performance every 18 months. This raw capability is provided without any investment from the ACS program, but component architectures are required that are capable of delivering this performance to an application. In a typical FPGA device on the market today an 8-bit operation consumes about 100 gates. A 50,000 gate device clocked at 40 MHz should therefore be able to provide 20 Mops or about 100x the performance of a state of the art microprocessor. Actual results are often far short of this goal with designs able to utilize perhaps 25% of the available gates at 10% of the maximum clocking rates before optimization. Results vary widely but fall far short of the maximum available performance.

While raw performance is available to produce single devices operating at teraop levels by the end of the century, dramatic changes in architectures are required to deliver this performance outside the device.



The ACS program is organized into the three levels of configurable components, development tools, and user-level software. Each of these areas is critical to the success of this technology. Capabilities and focus topics are identified in each of these ACS areas.



# Adaptive Computing Systems Potential Collaborators and Testbeds (Will Be Down-Selected)



- ATR testbed (STARLOS, M-STAR): Sandia, DARPA ISO
- New algorithms OPAL (Optimized Portable Applications Library) initiative: DARPA DSO
- INFOSEC: NSA
- Radar signal processing, AEGIS testbed: NSWC
- Sensor applications: DARPA STO
- RASSP, packaging, DASP, smart modules: DARPA ETO
- Embedded, Survivability, Microsystems, Active Nets: DARPA ITO, Rome Labs
- New Millennium and REE programs: NASA
- Space applications: ONR, JPL
- Sonar processing testbed: NUWC
- ARL federated lab advanced sensor and communications testbeds

The ACS program will be organized to closely coordinate technology development with Defense and Government customers to accelerate technology insertion.

Applications span sonar processing, space computing, information security, signal processing, active nets, and communications.



### **Technology Transfer Approach**



### **Defense Testbeds**

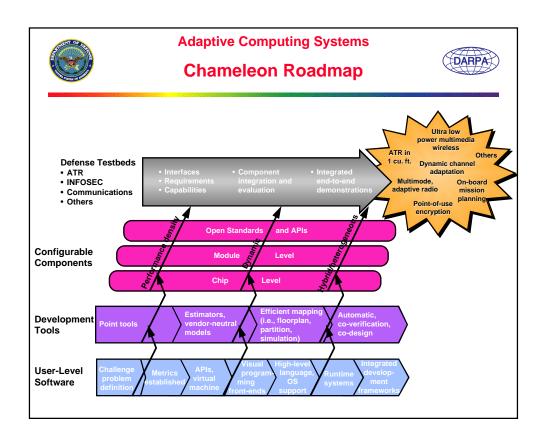
- Highly-leveraged
- Customer-owned
- Chameleon augmented (i.e., offset incremental cost/risk of insertion and community access)
- Provide application, domain-specific expertise
- Provide access to databases, systems, algorithms, etc.
- Validate Chameleon technology in stressing environments
- Accelerate technology transfer to Defense
- Spans application areas (e.g., information security, communications, signal/image processing)

#### **Defense Challenge Problems**

- Unclassified, quantitative, domain-specific characterizations of future Defense needs
- Define a capability within a mission context
- Infer technology requirements to drive research
- Does not adopt problem ownership
- Created by passionate defense customers/mentors

To specifically encourage technology transfer to Defense, two mechanisms will be established. ACS will coordinate with existing Defense and Government testbeds for the purpose of evaluating ACS technology in a mission context. Several testbeds have been identified and mechanisms for transfer are being established. Additional testbeds are sought in various application areas. Testbeds should be in areas of relevance to Defense and be owned by passionate users.

In addition to testbeds, a series of "challenge" problems is being established. These challenge problems may be associated with a testbed but not necessarily so. Challenge problems are unclassified characterizations of desireable future levels of functionality in areas of Defense interest. Challenge problems define a future capability in terms that constitute an ACS challenge for which progress can be measured and for which someone cares about the answer. Challenge problems must also have a passionate owner that will interface with the research community to define the problem, work with the community, and assist with insertion of results. Several challenge problems are already being established but ACS seeks additional challenge problems.



While ACS is organized into three areas of research the goal of ACS is to impact Defense-critical application areas with unprecedented levels of adaptability and performance. This chart shows the timeline and flow of technology across the research levels and out through the testbeds. The timeline spans three general phases of development. Performance/density represents the first phase of component development focused on improvements in these parameters. The second phase of development will exploit the dynamic nature of computing and the third phase will develop new classes of architecture that are hybrid mixes of DSP, microprocessor, custom, and configurable as well as entirely new offerings.

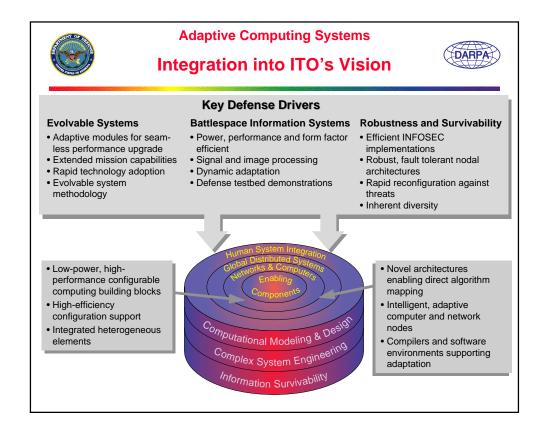


### **Quantitative Goals**



- Reduced power/gate penalty over custom 10x → 1.2x
- 10-100x reduced power/gate
- 20x denser, 10x faster
- 10x reduced configuration overhead
- 1,000,000x reduction in reconfiguration time: msec → nsec
- Hybrid architectures
  - 1x in performance of over custom ASICs
  - 10x in performance over contemporary DSP
  - 100x in performance over contemporary microprocessor
- 10x productivity improvement: 15,000 → 150,000 gates/week
- 100x reduction in compilation time
- Automatic mapping of 500,000 gates

The ACS program has established a set of program goals that attempt to convey the breadth of investment and magnitude of anticipated improvements. This list of goals and metrics will continue to evolve as our understanding of this field grows and as the research community responds to the challenge and responds to common goals and shared technology.



The ACS program supports the Information Technology Office vision of providing an integrated information technology suite that is scalable, survivable, and adaptable. The key Defense drivers of Evolvable Systems, Battlespace Information Systems, and Robustness and Survivability are each directly addressed by the ACS technology approach. ACS provides the enabling technology for truly adaptable information system solutions across a broad range of Defense challenges.